



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Large application of Kenneth E. Knapp et al.

Serial No.: 09/500,380

Filed: February 8, 2000

Examiner: C. Renner

Atty. Docket No.: RR-1645

GAU: 2652

For: SUBMICRON TRACK-WIDTH POLE-TIPS FOR ELECTROMAGNETIC
TRANSDUCERS

October 16, 2003

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

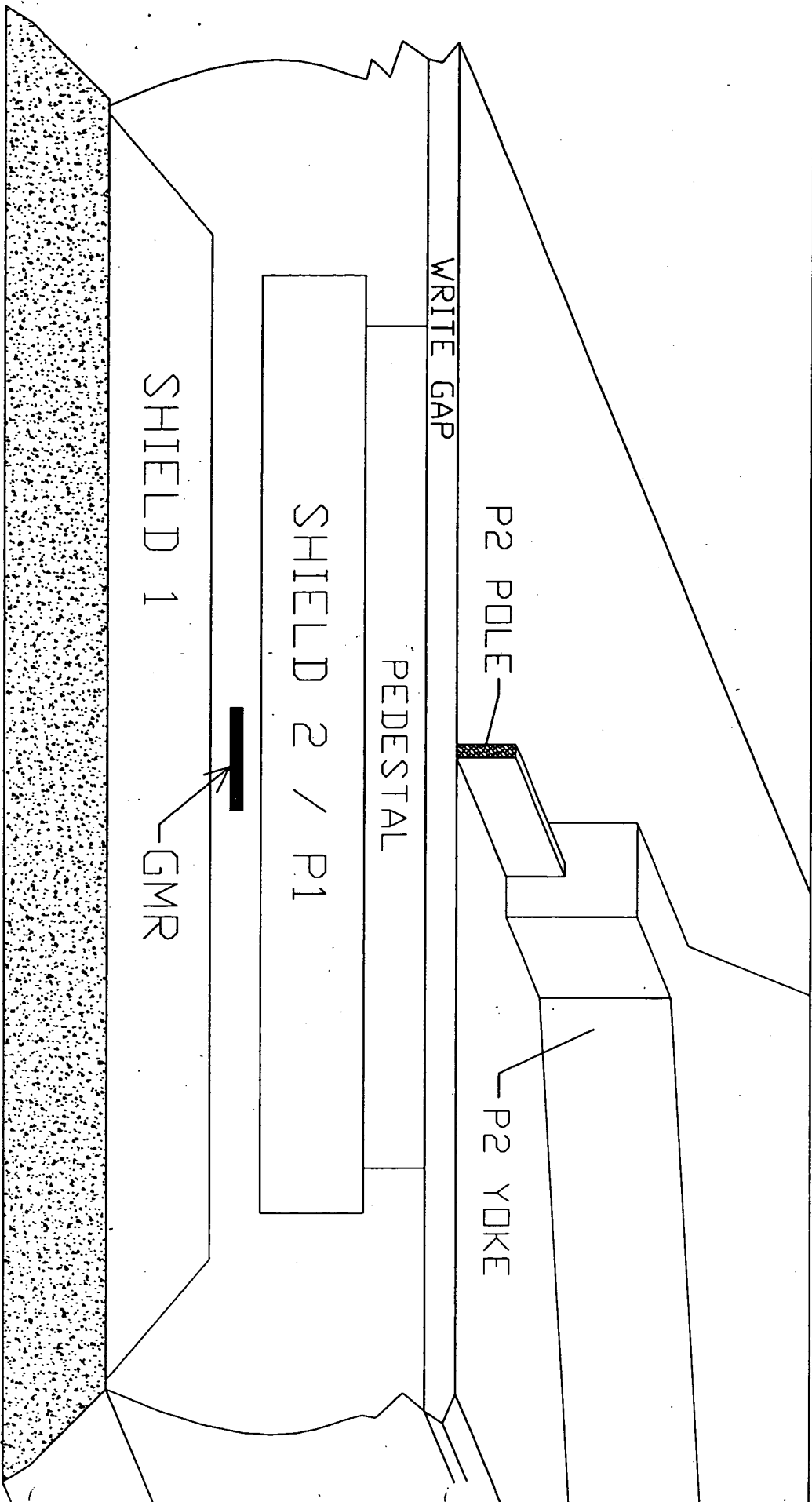
Declaration of Kenneth E. Knapp
Under 37 C.F.R. § 1.131

I, Kenneth E. Knapp, declare:

1. I am an inventor of the invention claimed in U.S. Patent Application Serial Number 09/500,380, including independent claim 1.
2. Attached is a copy of an eight-page set of drawings entitled: "METHOD OF DEFINING SUB-0.5um NARROW TRACK," dated 5-29-99. These drawings show that I conceived the invention defined by independent claim 1 of the above-referenced patent application at least as early as May 29, 1999.
3. Patent protection was diligently pursued from on or before August 4, 1999 to the filing of U.S. Patent Application Serial Number 09/500,380 on February 8, 2000.
5. The above described conception and invention occurred in the United States, in and around Fremont, California.
6. I hereby declare that all statements made herein of my own knowledge are

true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001, Title 18, of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: October 16, 2003 Kenneth E. Knapp
Kenneth E. Knapp



"METHOD OF DEFINING SUB-0.5um NARROW TRACK"

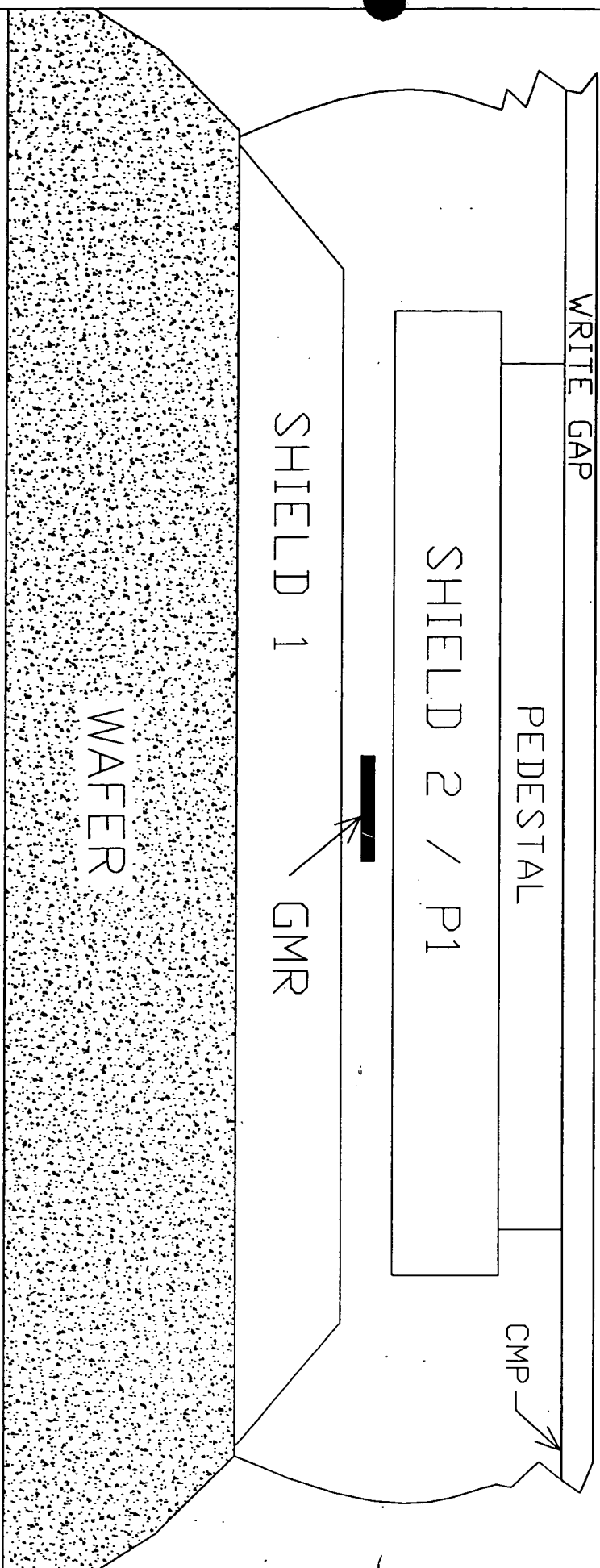
II

ABS VIEW OF NEW INVENTION

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READ-RITE Corporation MASK DESIGN DEPT. FAX 510-683-7065			
TITLE: "METHOD OF DEFINING SUB-0.5um NARROW TRACK"			
SIZE B	STITCH	DWG FILE	REV
SCALE	SHEET 1 OF 9		

Sheet III

PROCESS STEPS:

- STEP 1) STANDARD 12 GBIT PROCESS TO PEDESTAL CMP
 STEP 2) DEPOSIT WRITE GAP, PROCESS COIL AND 12 (NOT SHOWN)

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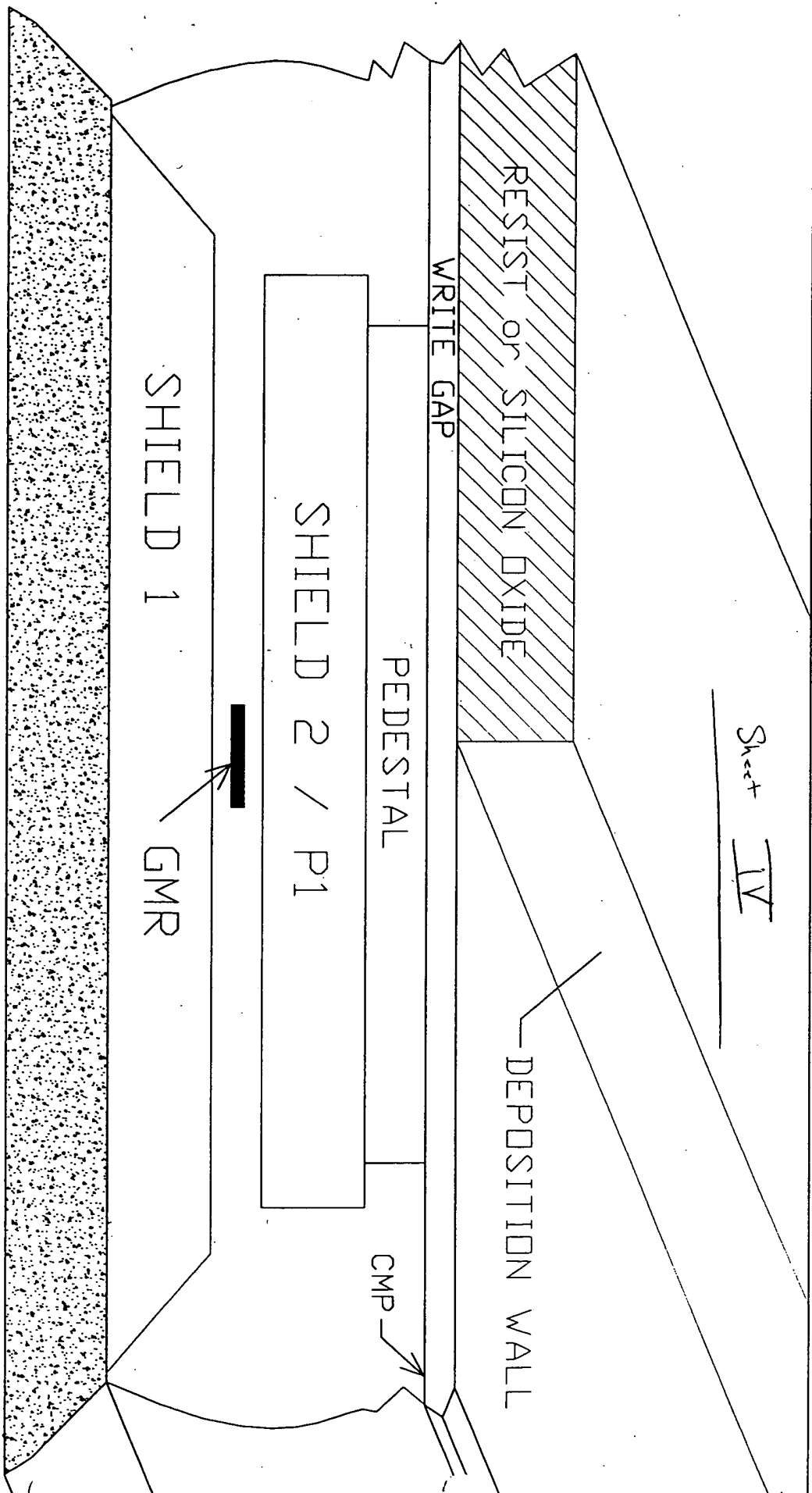
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METHOD OF DEFINING SUB-0.5um NARROW TRACK"

SIZE	SYMBOL	DWG FILE	REV
B			
SCALE	SHEET 2 OF 9		

Sheet IV



PROCESS STEPS:

STEP 3) CREATE PHOTORESIST OR SILICON DIOXIDE WALL

Forrest
11/11/79

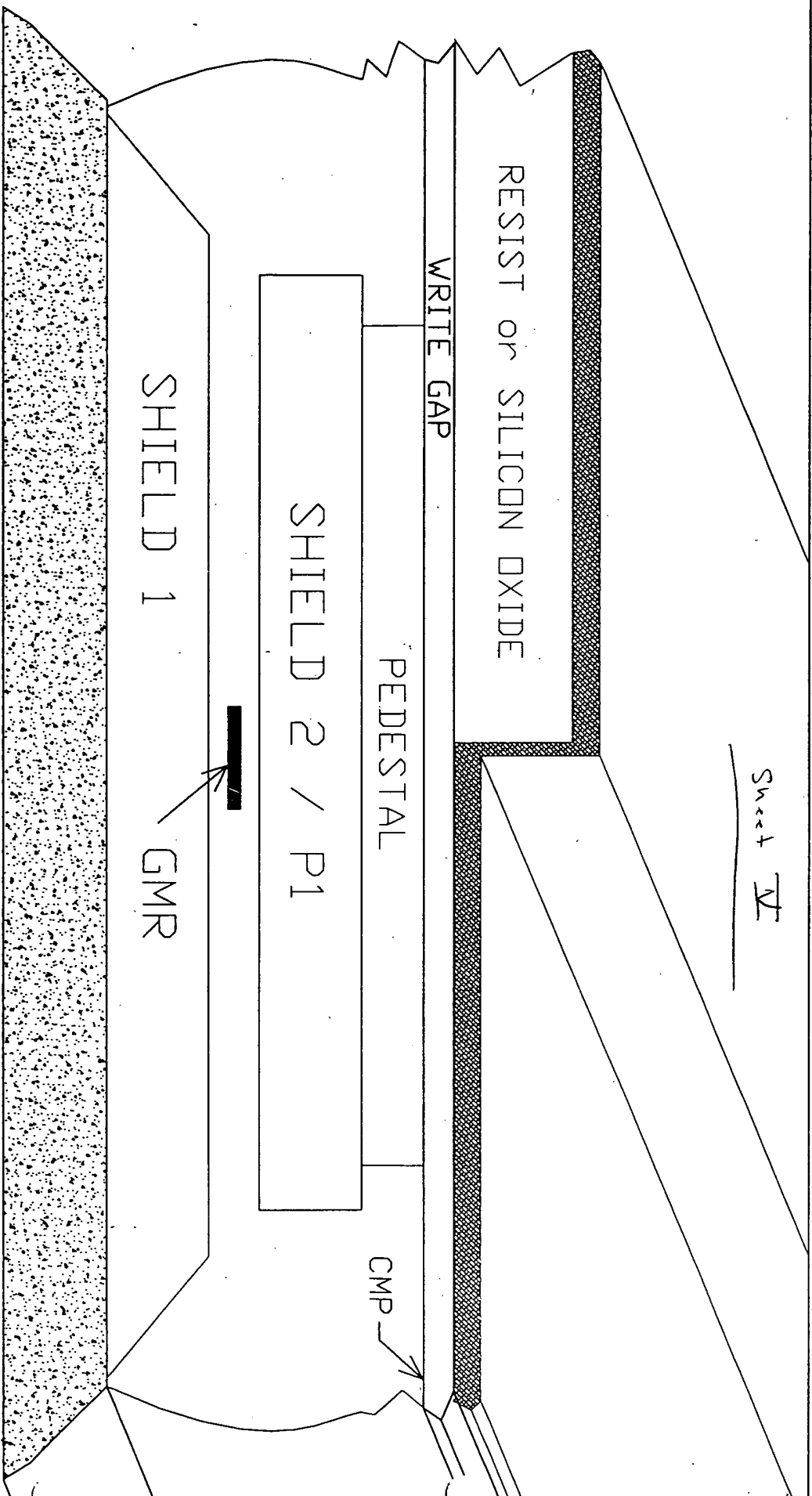
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REV	

SCALE	SHEET 3 OF 9
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Sheet 1



PROCESS STEPS:

STEP 4) DEPOSIT P2 MATERIAL

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METHOD OF DEFINING SUB-0.5um NARROW TRACK		
SIZE	SYSTEM	DWG FILE
B		
SCALE	SHEET 4 OF 9	

Sheet VI

RESIST OR SILICON OXIDE

WRITE GAP

PEDESTAL

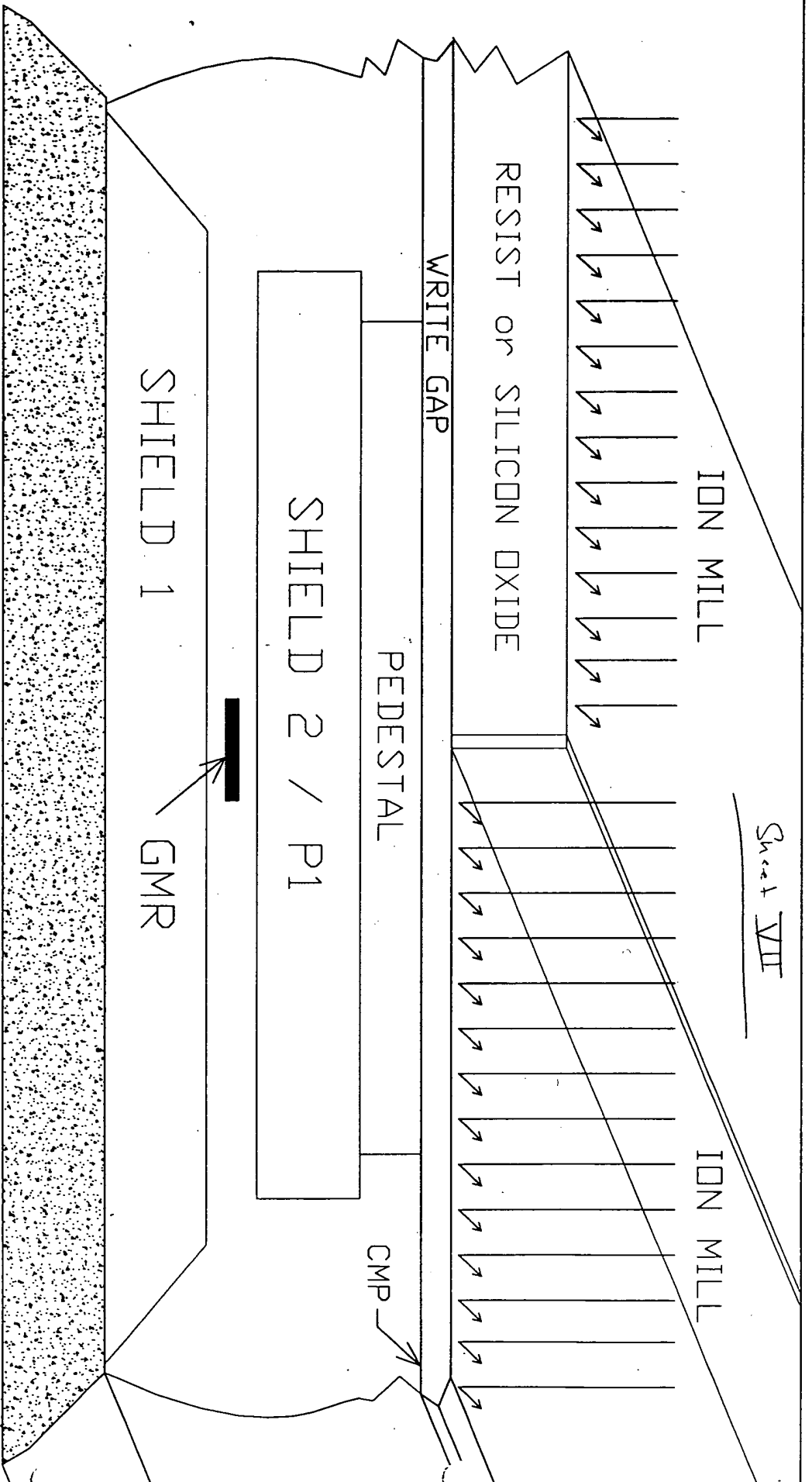
VERTICAL LAMINATIONS ARE POSSIBLE

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B		REV	
SCALE		SHEET 5 OF 9	

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PROCESS STEPS:

STEP 5) ION MILL TO CREATE THE P2 STRUCTURE

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SITE		REV	
B		SHEET 6 OF 9	

Sheet VIII

TRACK WIDTH

WRITE GAP

PEDESTAL

SHIELD 2 / P1

CMP

SHIELD 1

GMR

PROCESS STEPS:

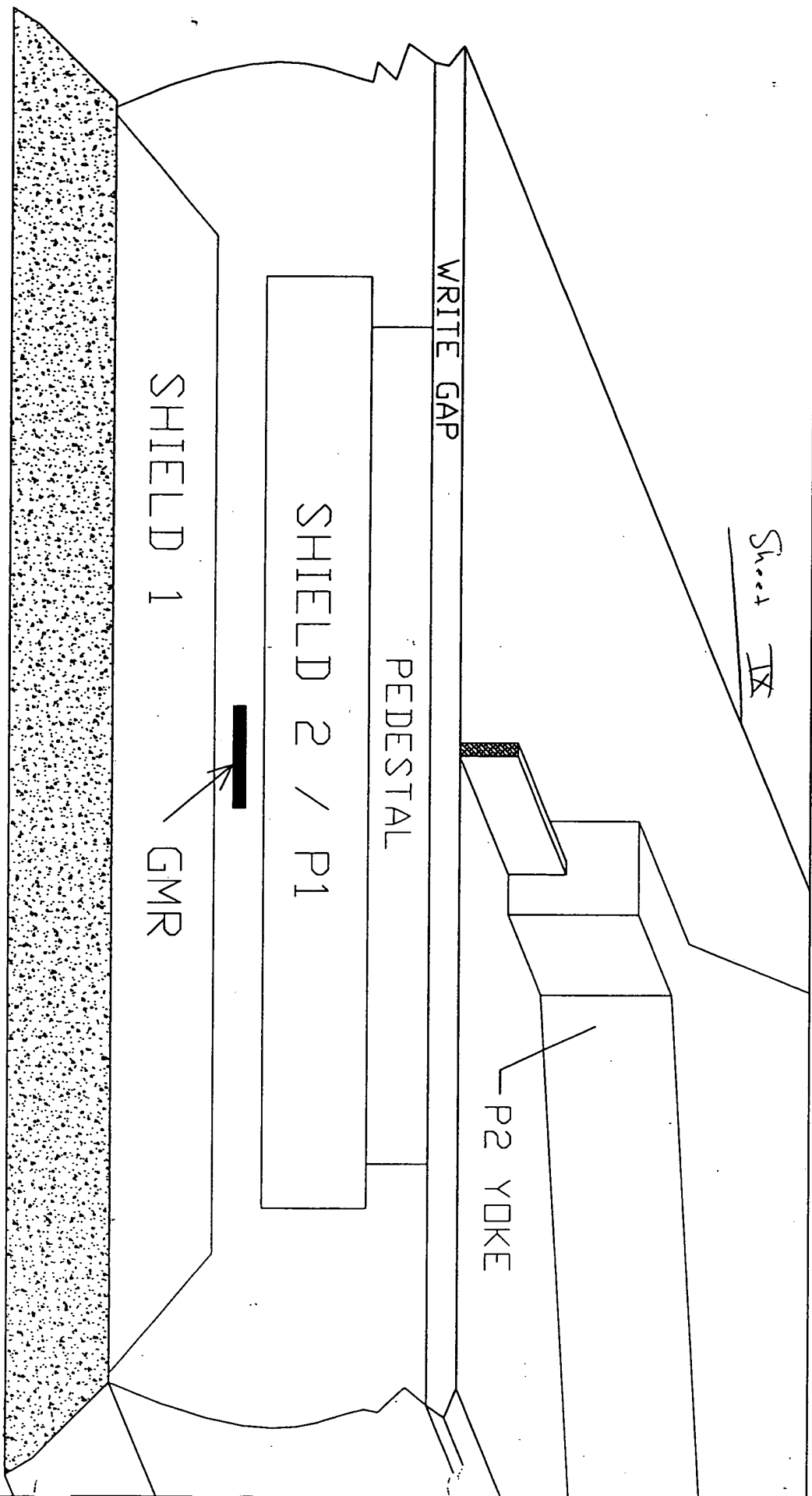
STEP 6) REMOVE RESIST OR SILICON DIOXIDE WALL

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SIZE	STITCH	DWG FILE	REV
B			
SCALE	SHEET 7 OF 9		

Sheet IX



PROCESS STEPS:

STEP 8) MASK AND PLATE P2 YOKE

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SHEET 8 OF 9